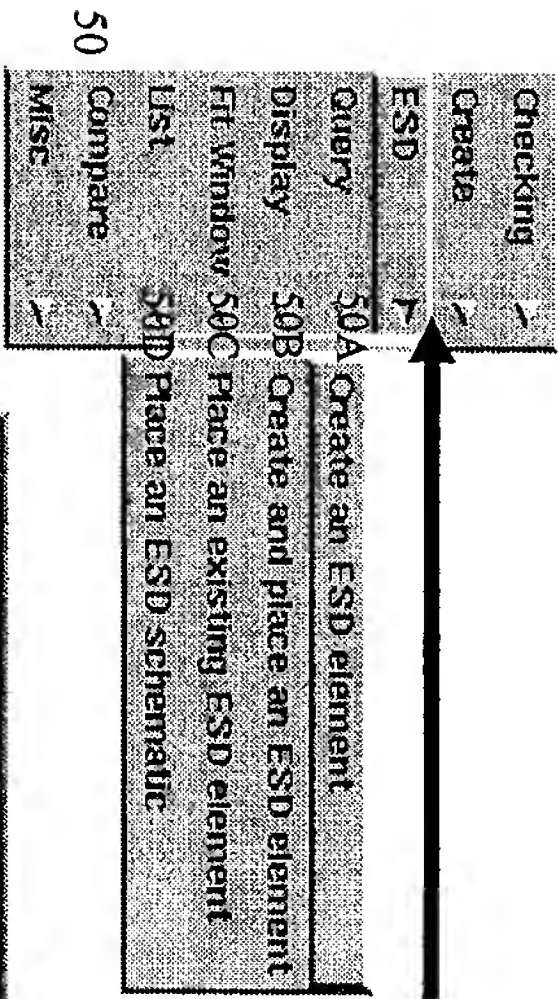


Figure 1



# P-Cell Network Creation and Placement

ESD Cell Type: 52

Function will: 54

Library Name: 56

Cell Name: 58

Number of Diodes (up): 60

Number of Diodes (down): 4

Cathodes per diode (up): 8

Cathodes per diode (down): 3

ESD schematic symbol:

# P-Cell Schematic and Graphical Representation

Figure 2

# Symbol Function

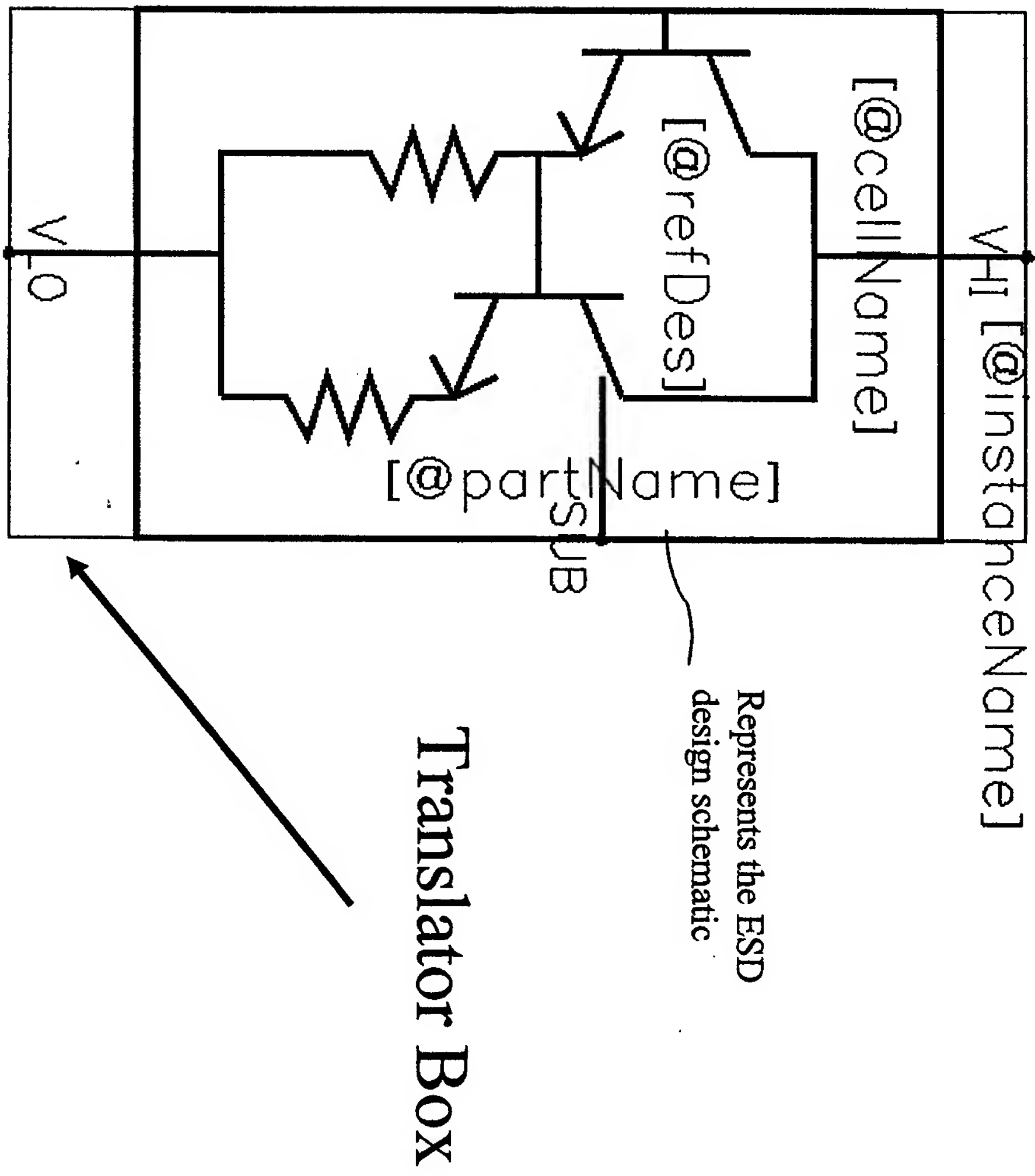


Figure 3

# Symbol Placement in Schematic Design

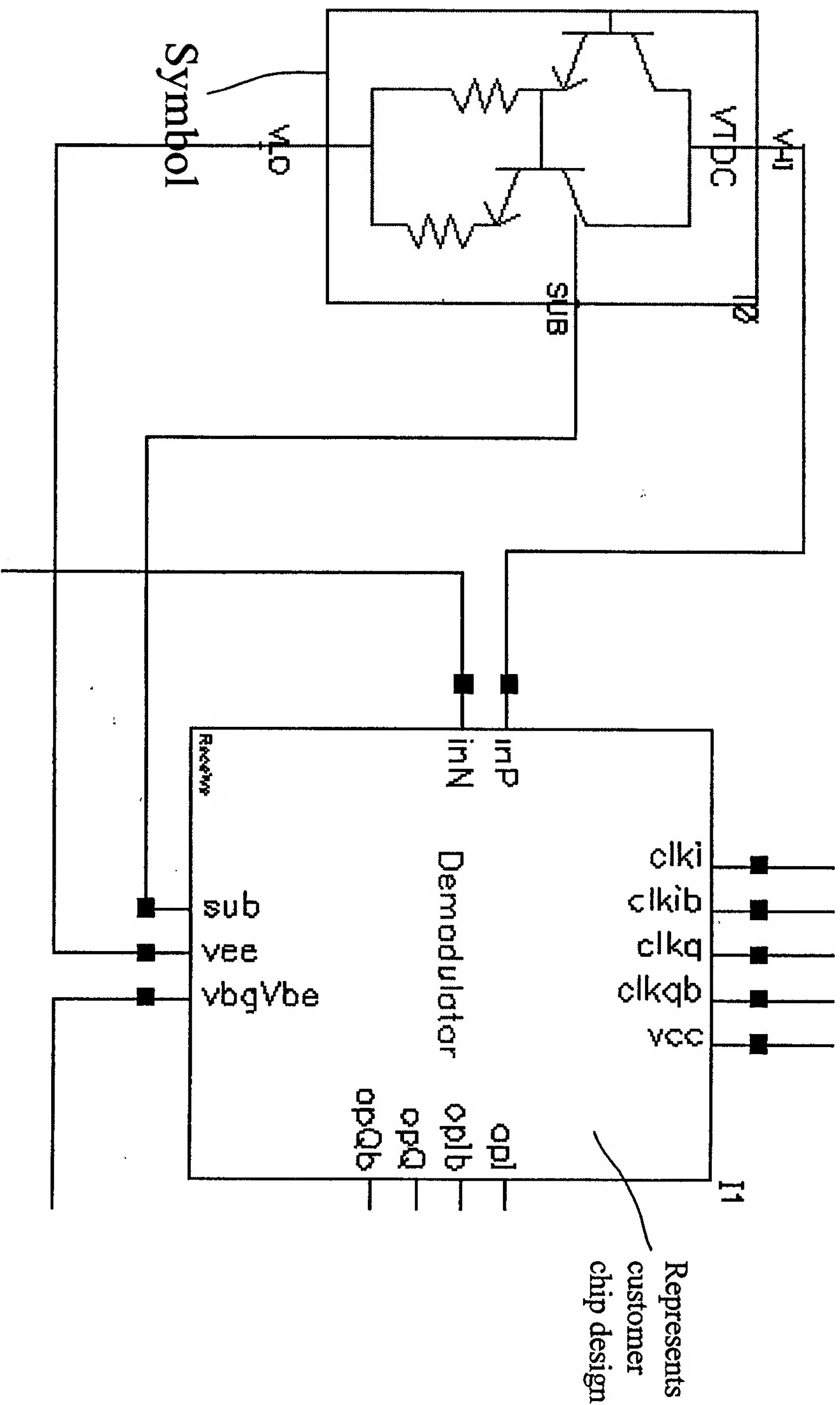


Figure 4

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# Schematic Representation of Hierarchical Circuit

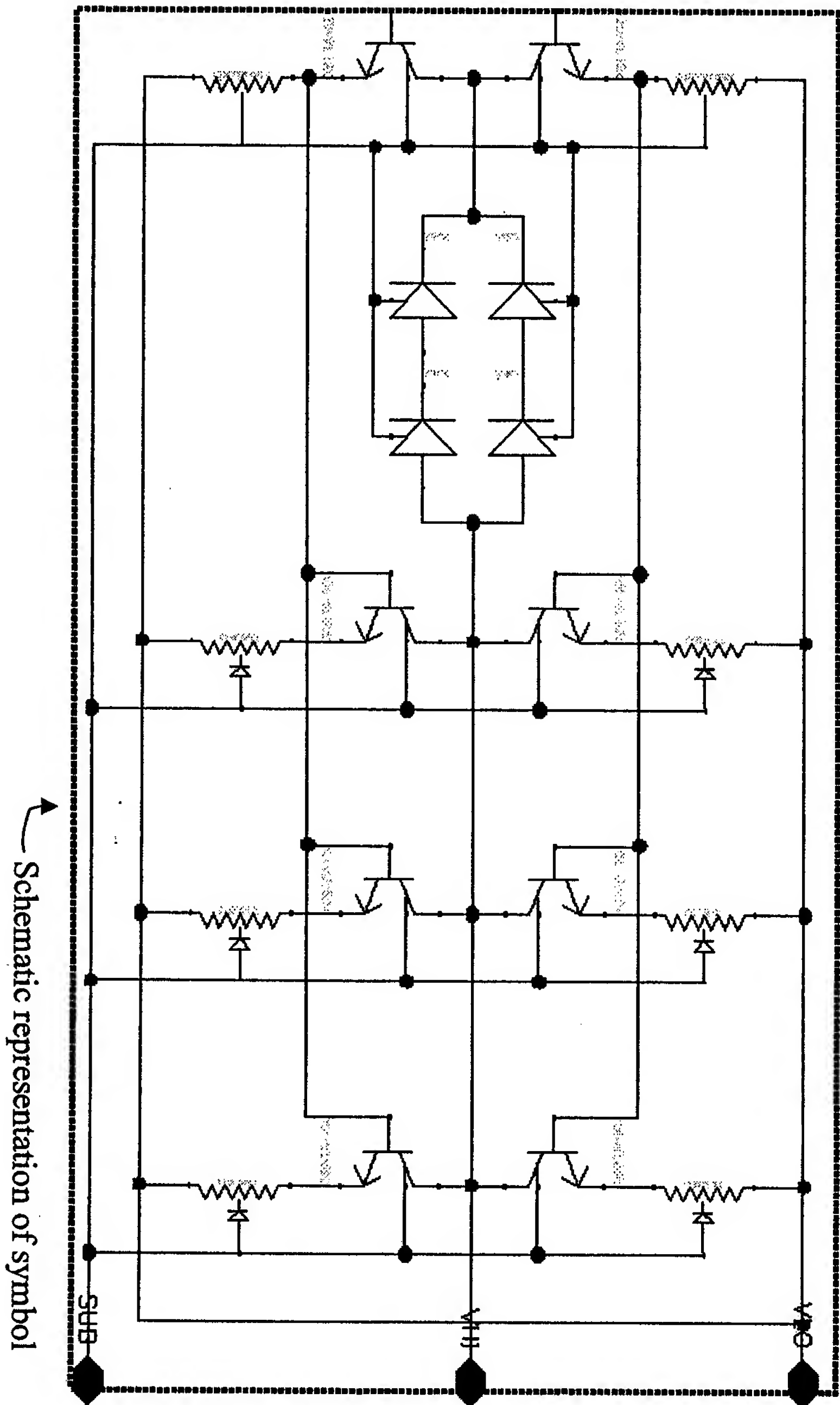


Figure 5

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# Hierarchical Schematic Placement in Design Schematics

Schematic representation of ESD

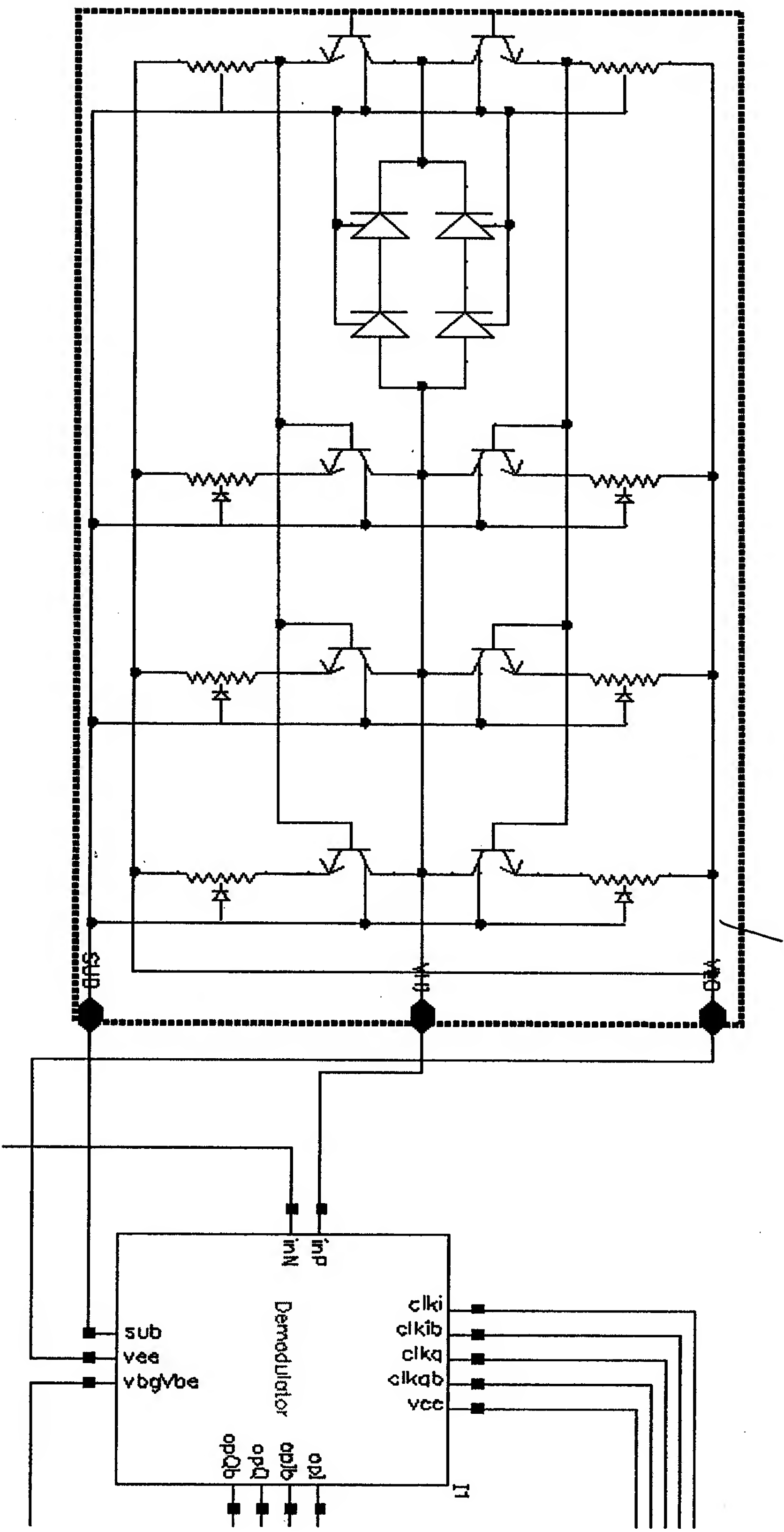
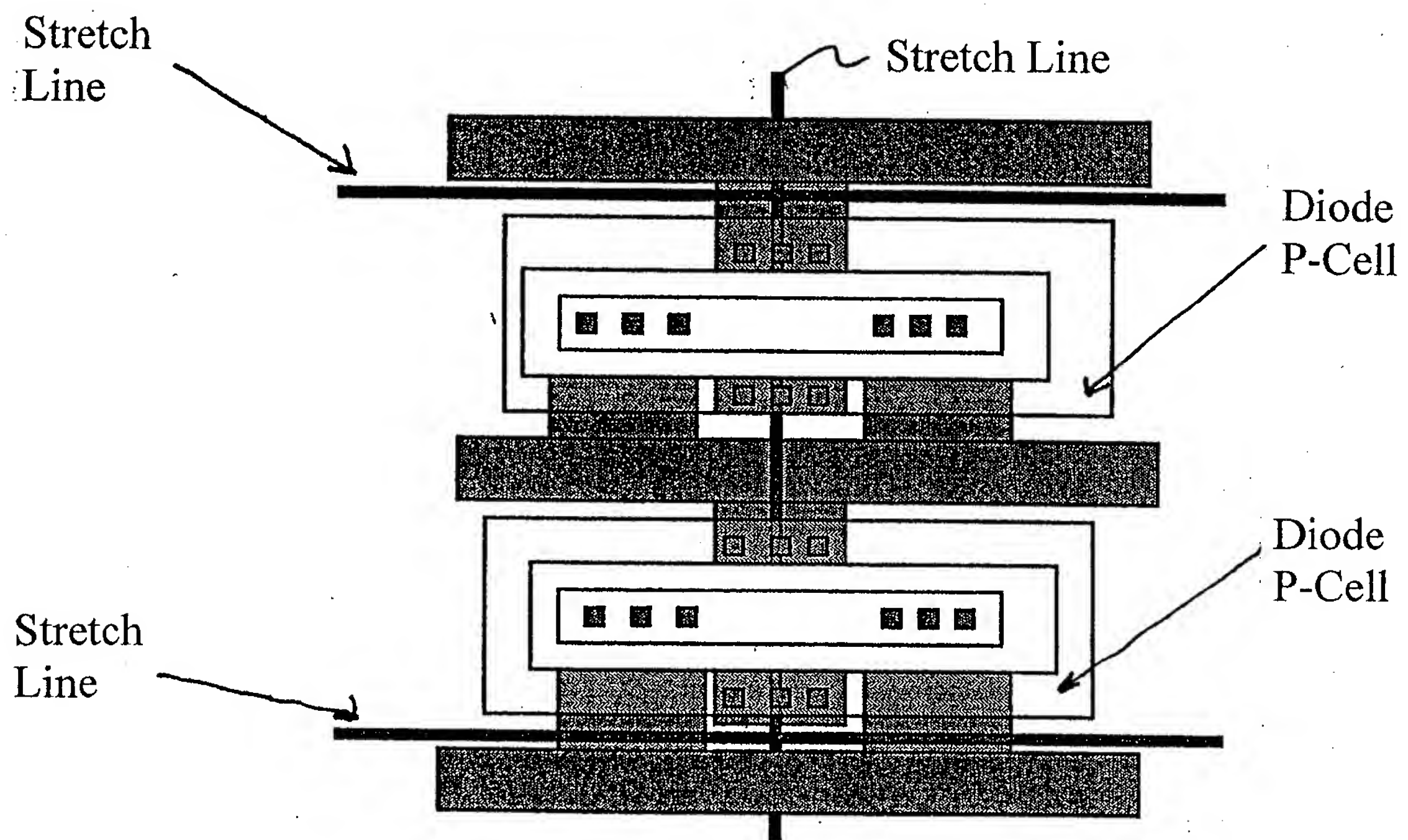


Figure 6

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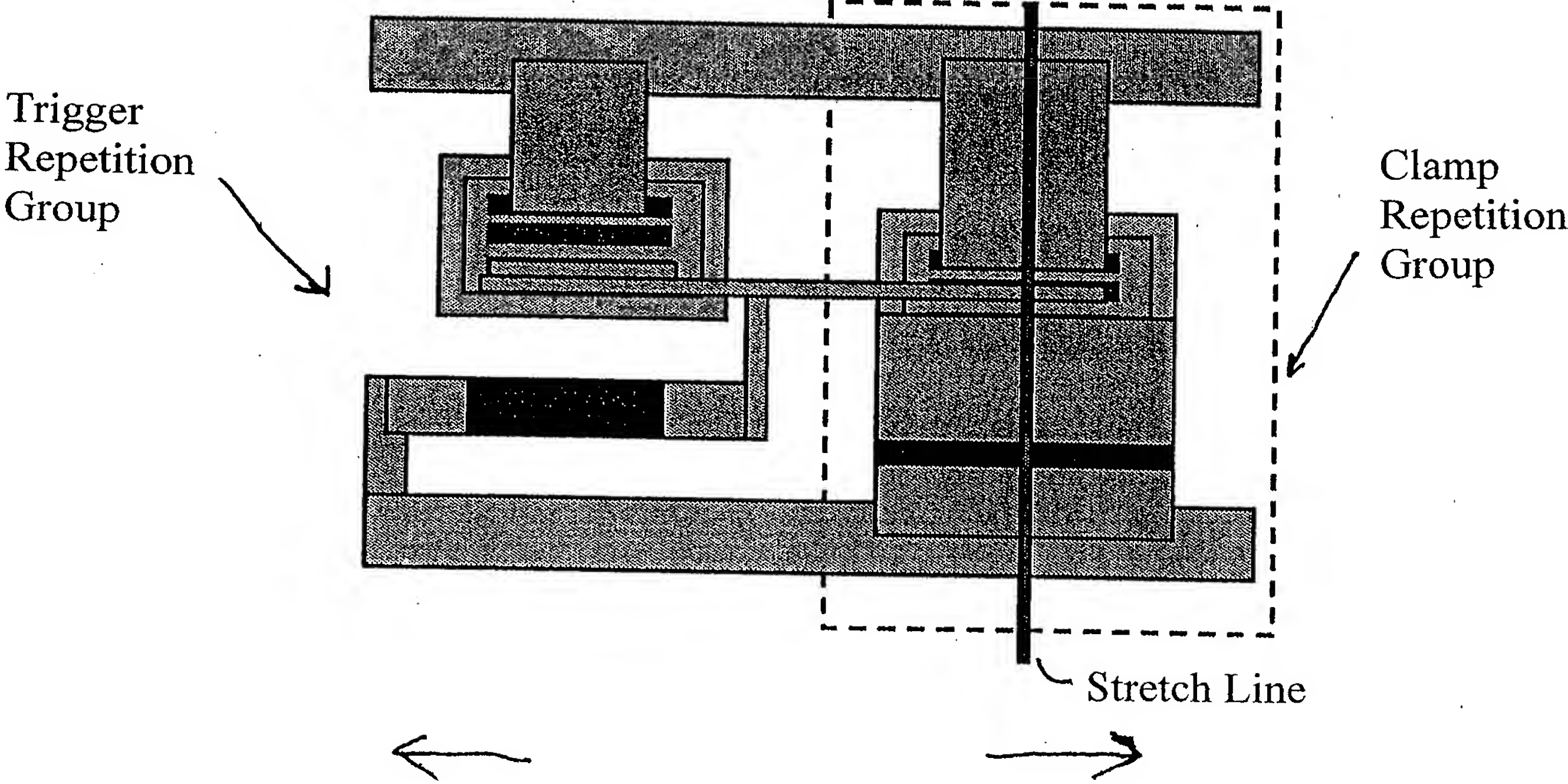
Figure 7





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Figure 8





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# Graphical Representation of Hierarchical Design

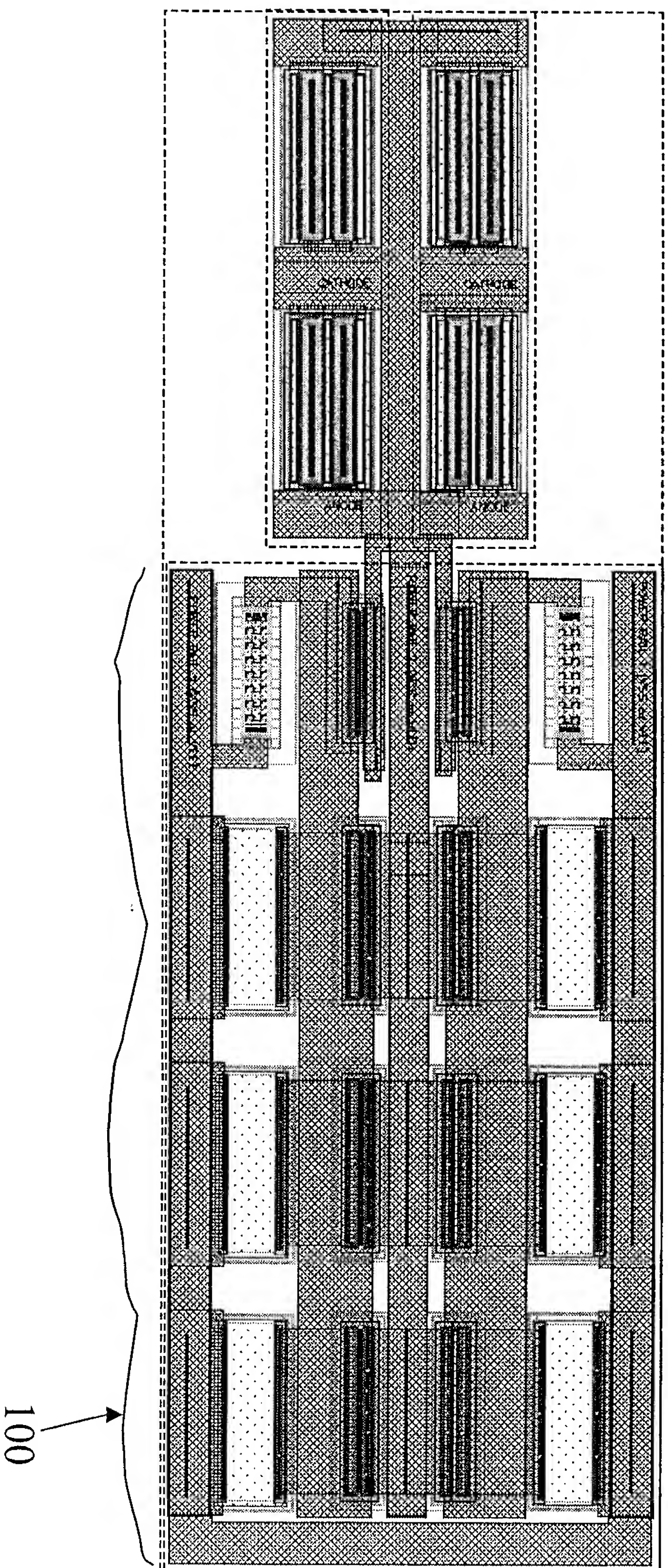
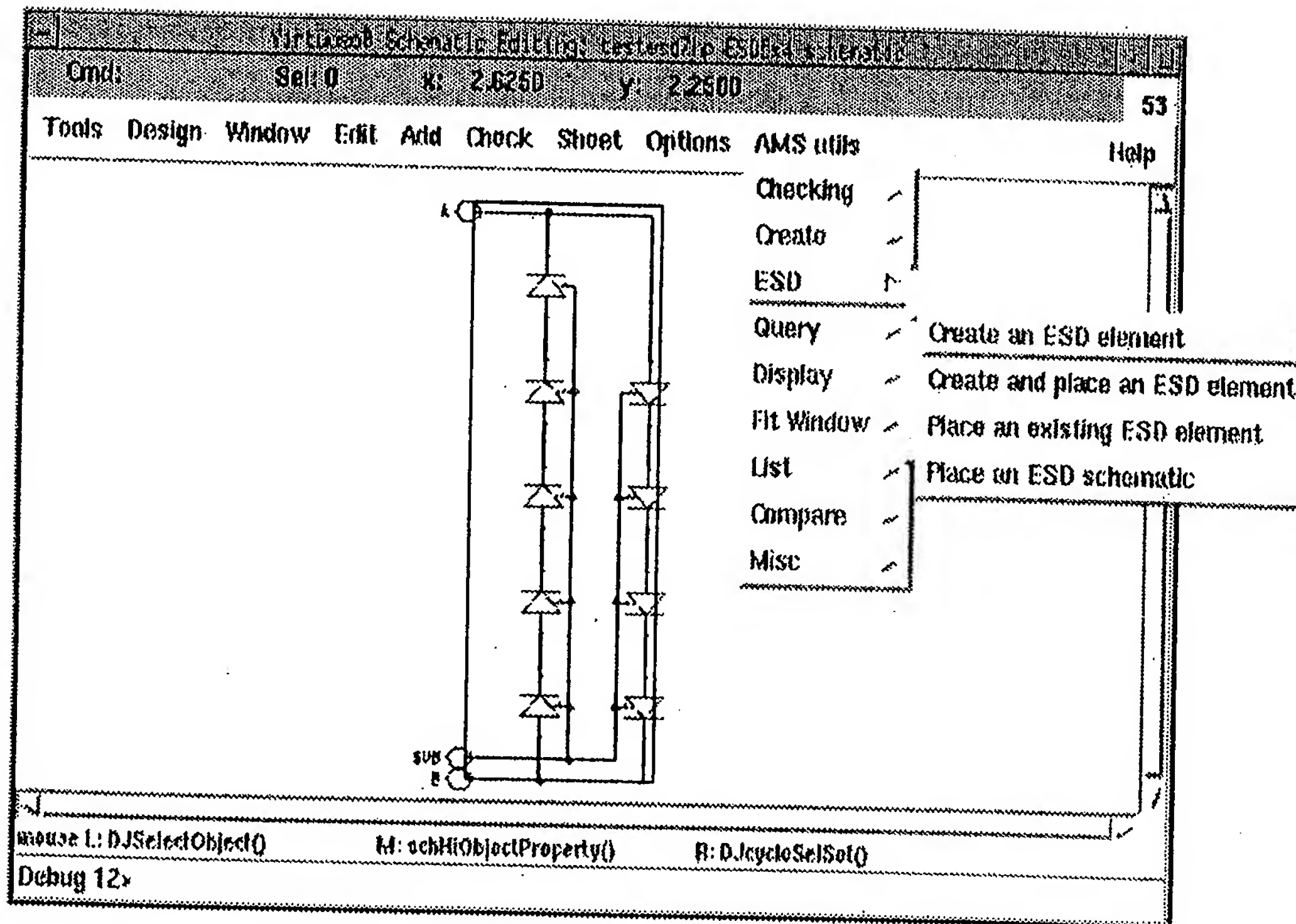


Figure 9

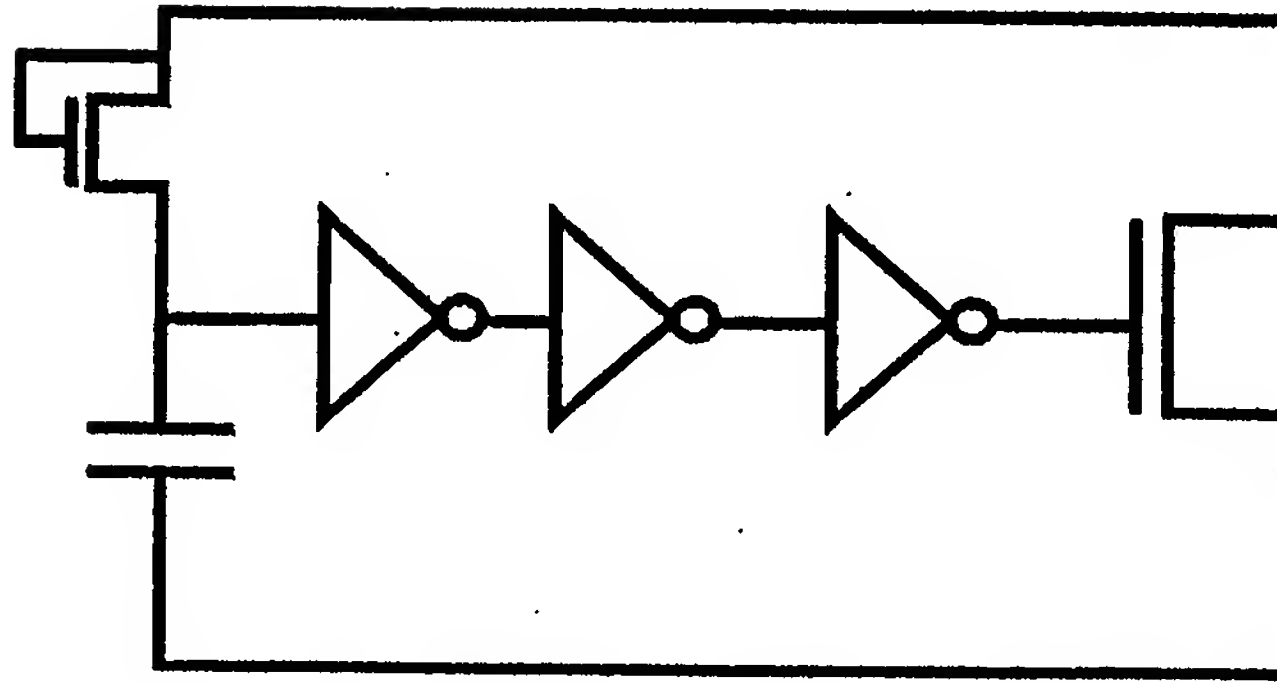
10/27

Figure 10



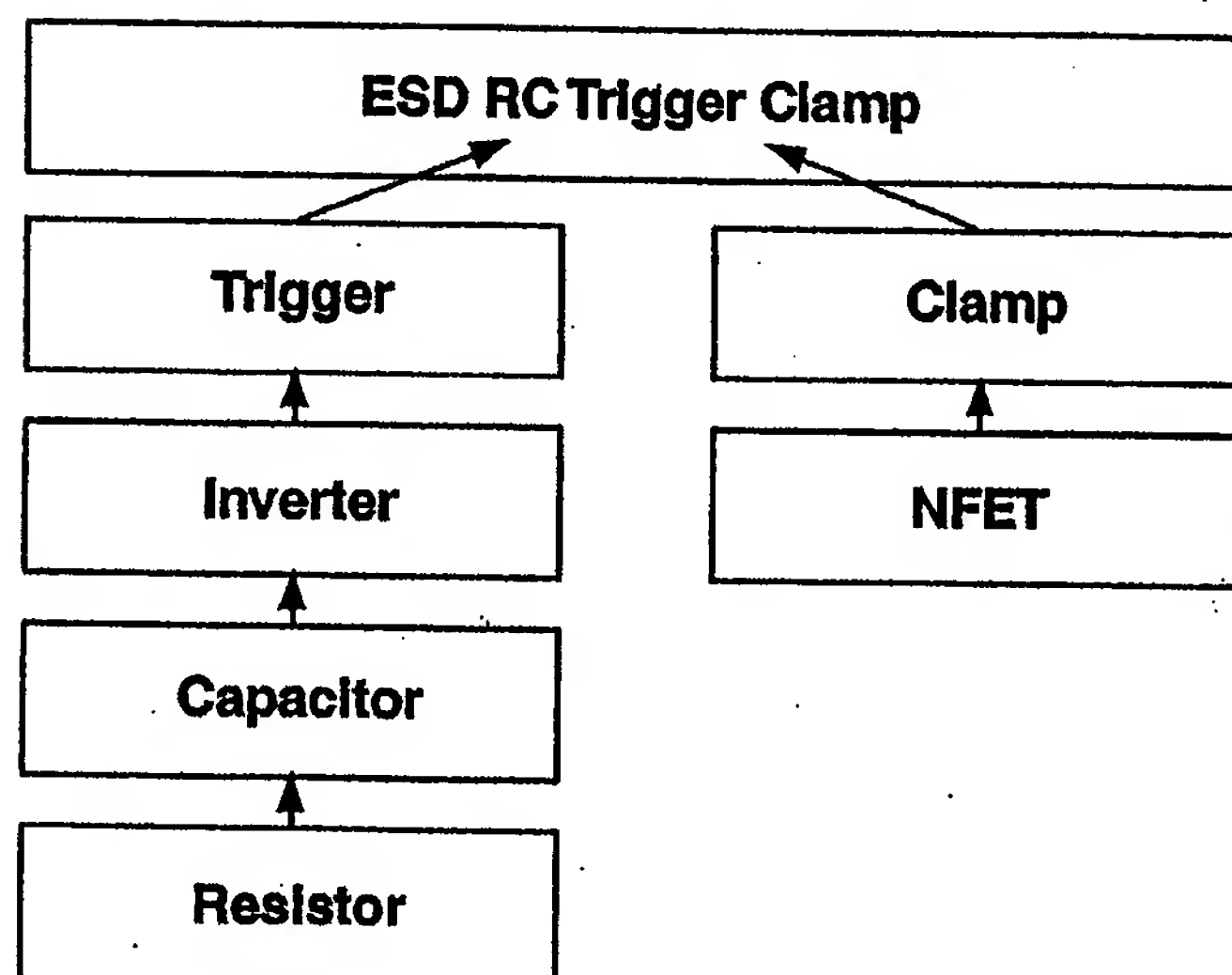
11/27

Figure 11



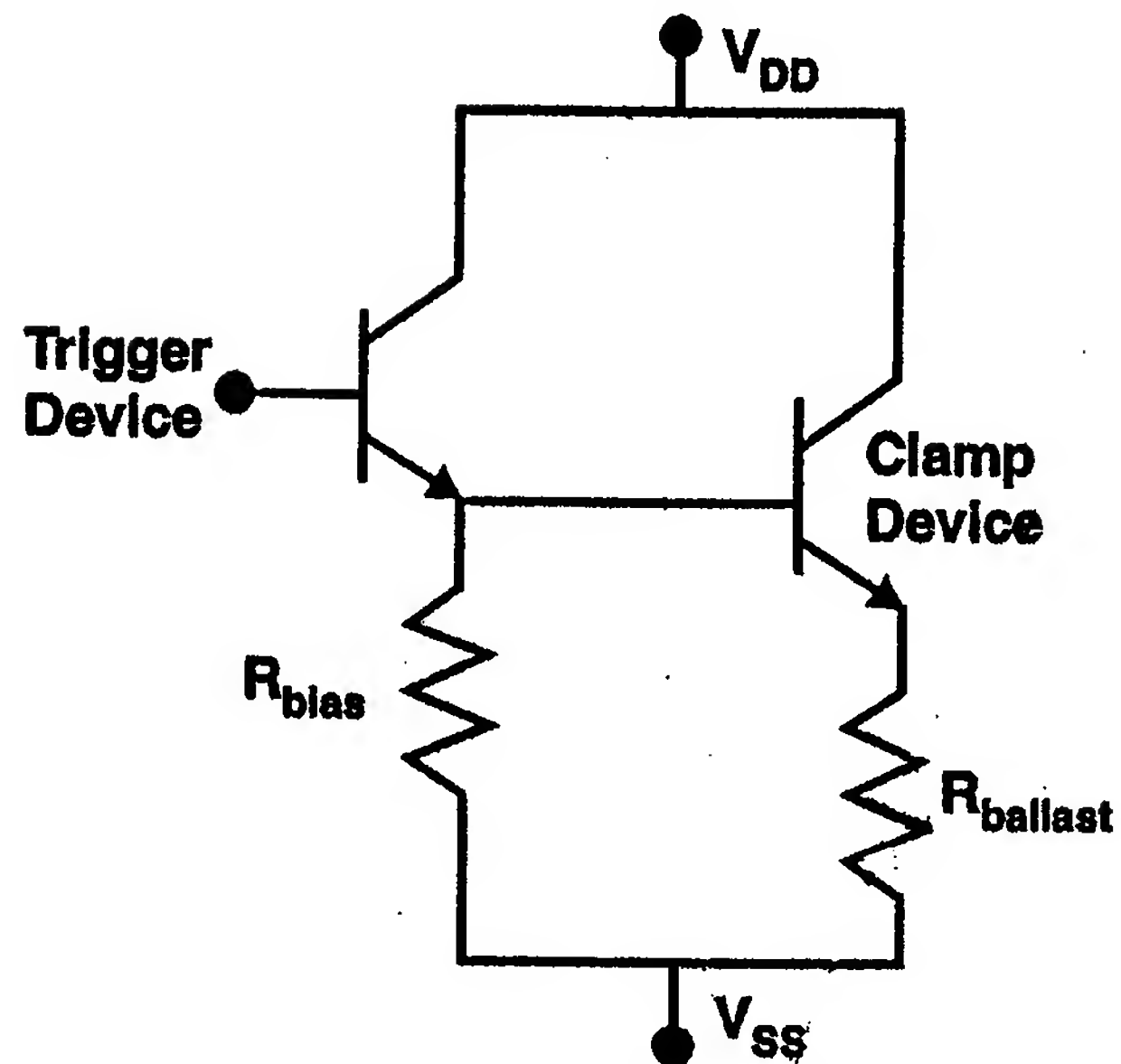
Symbol for D-C trigger clamp

Figure 12



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Figure 13



Symbol representation  
Variations of styles –  
for type of ESD element

Figure 14

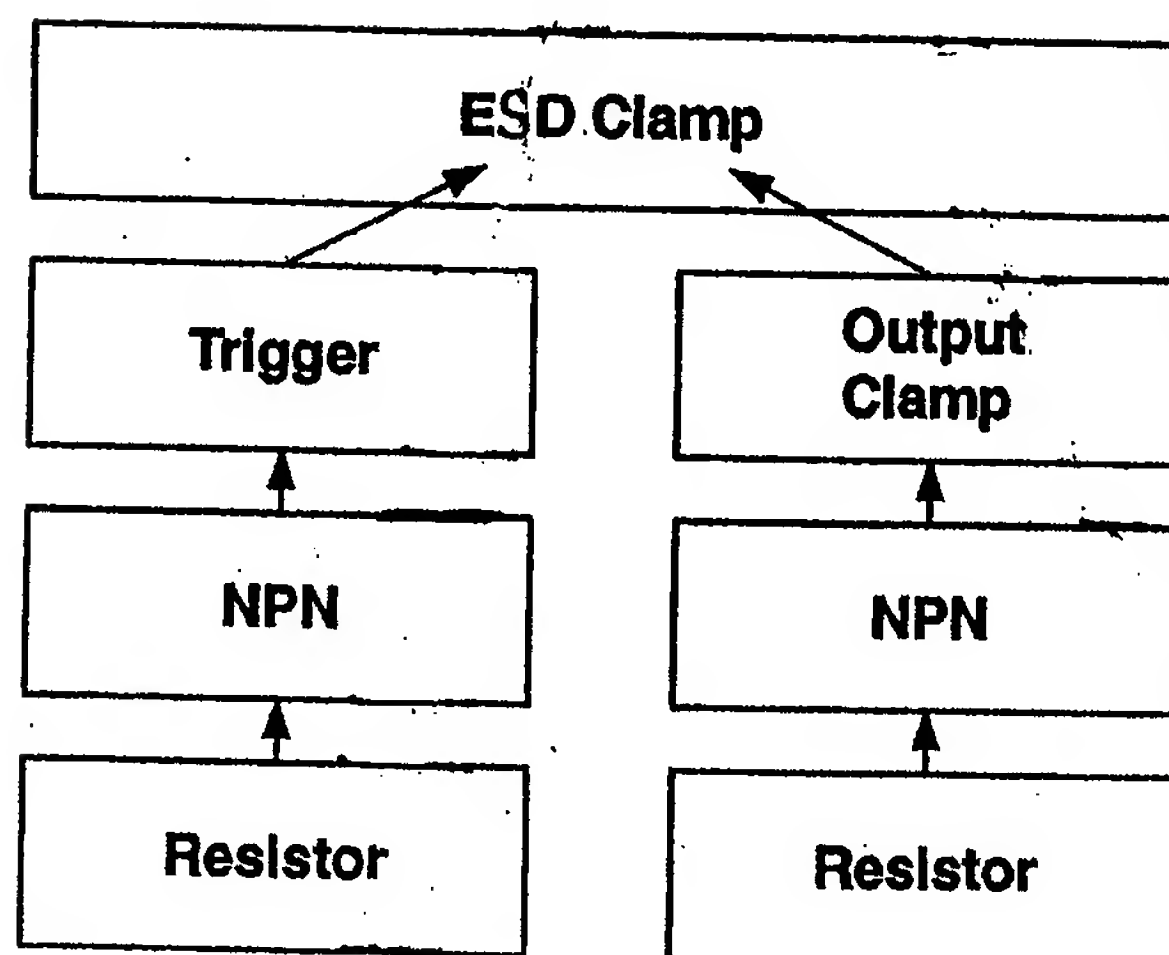


Figure 15

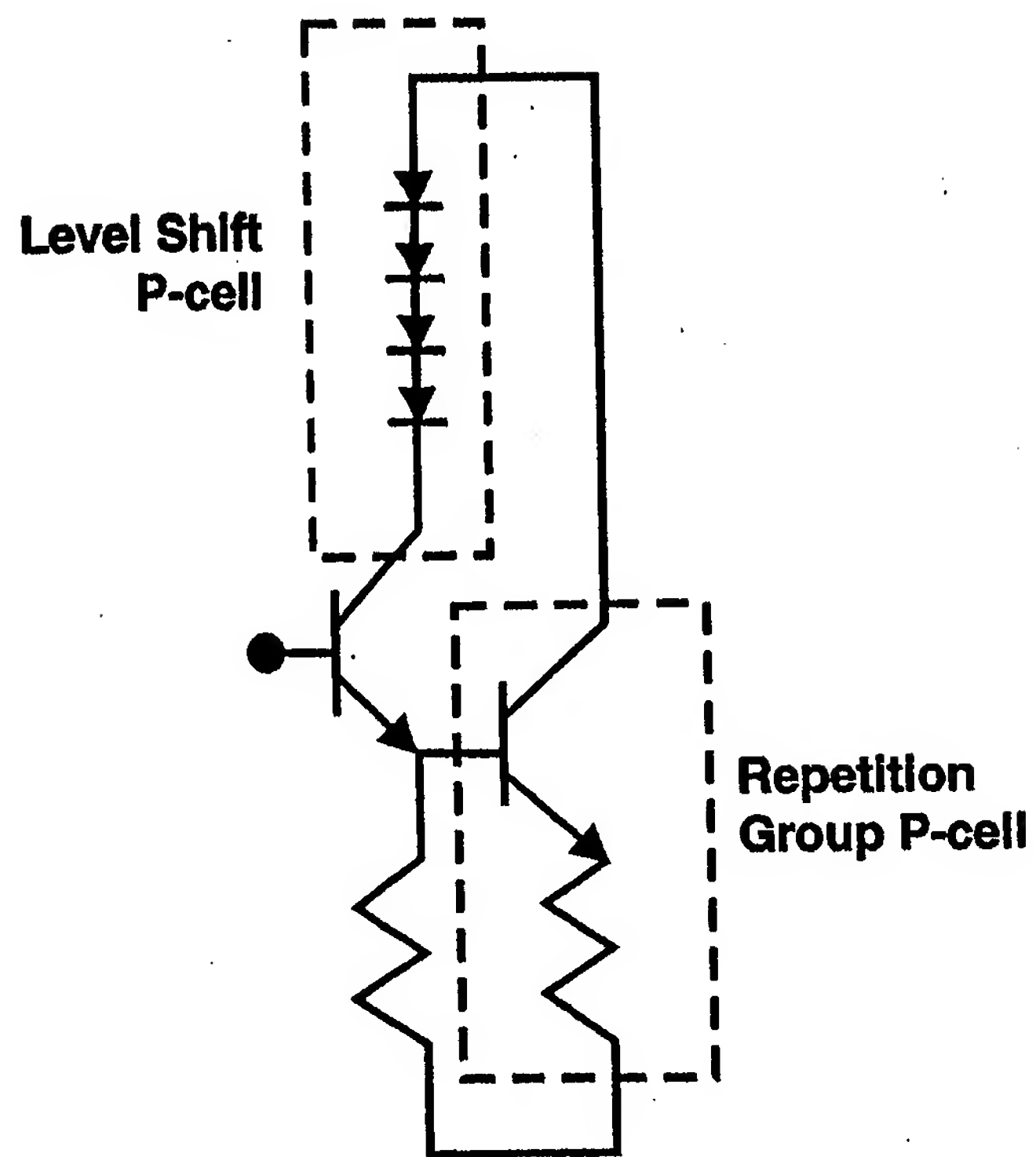
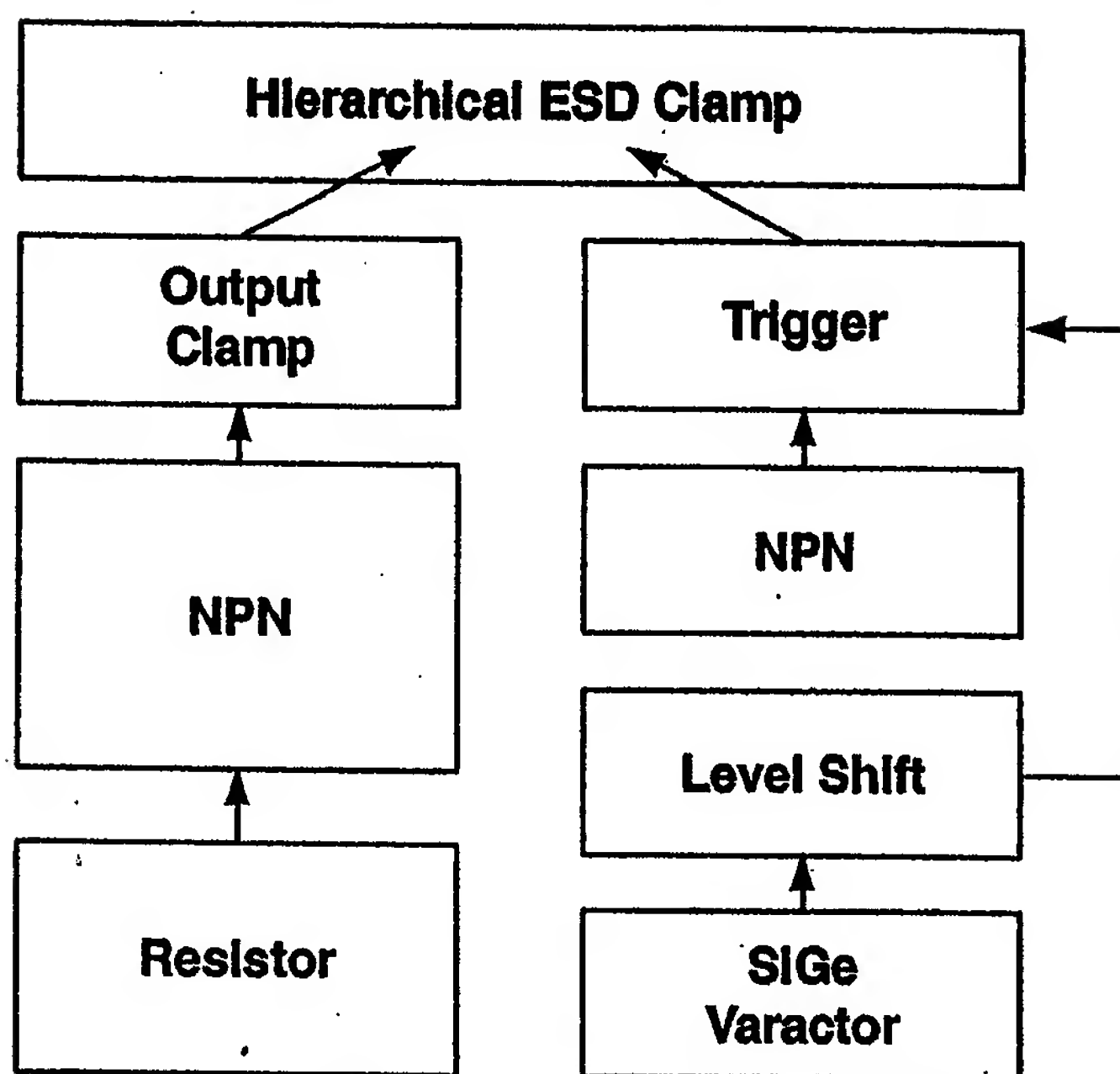


Figure 16





# Schematic Design System

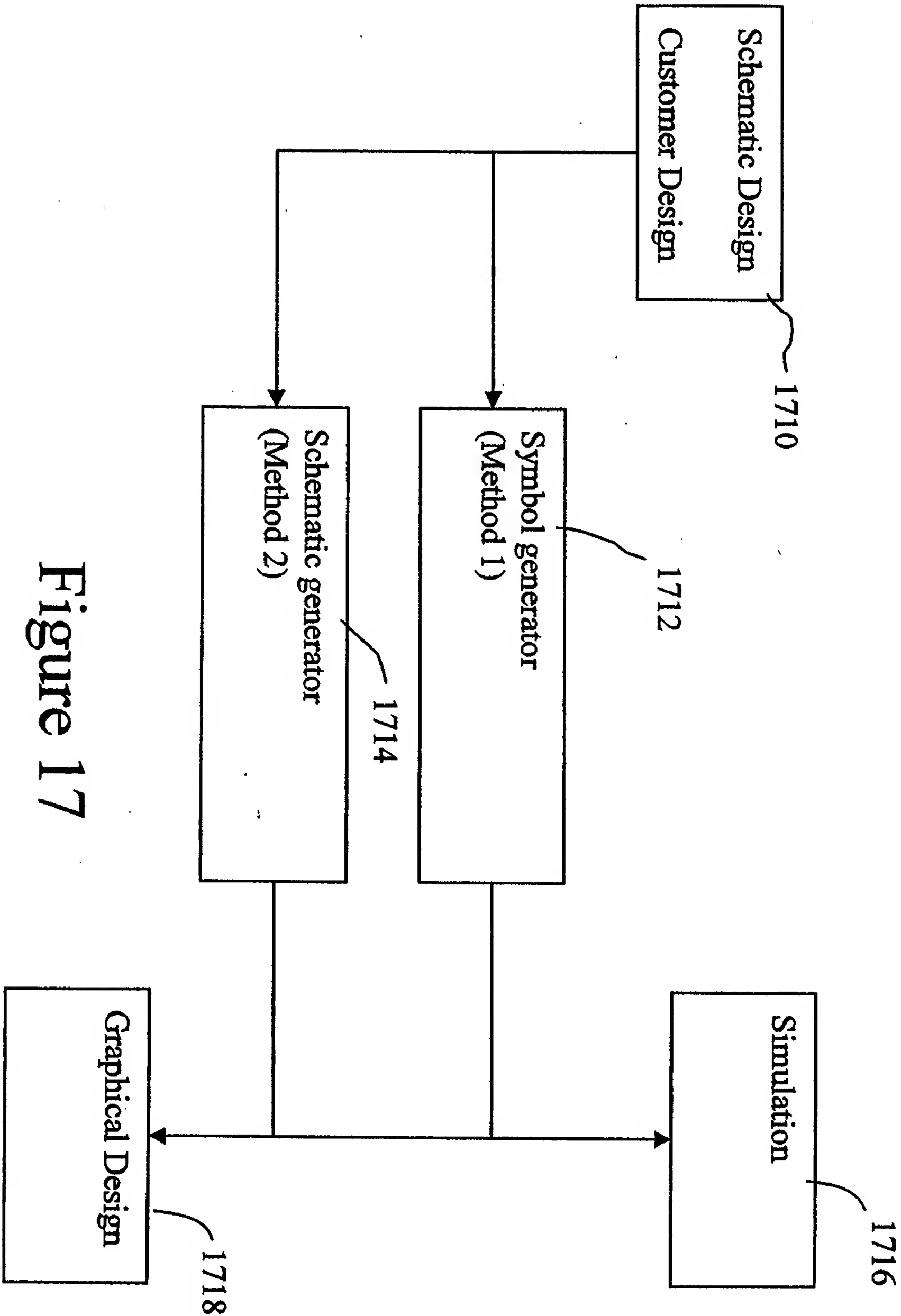


Figure 17

# Symbol and Schematic

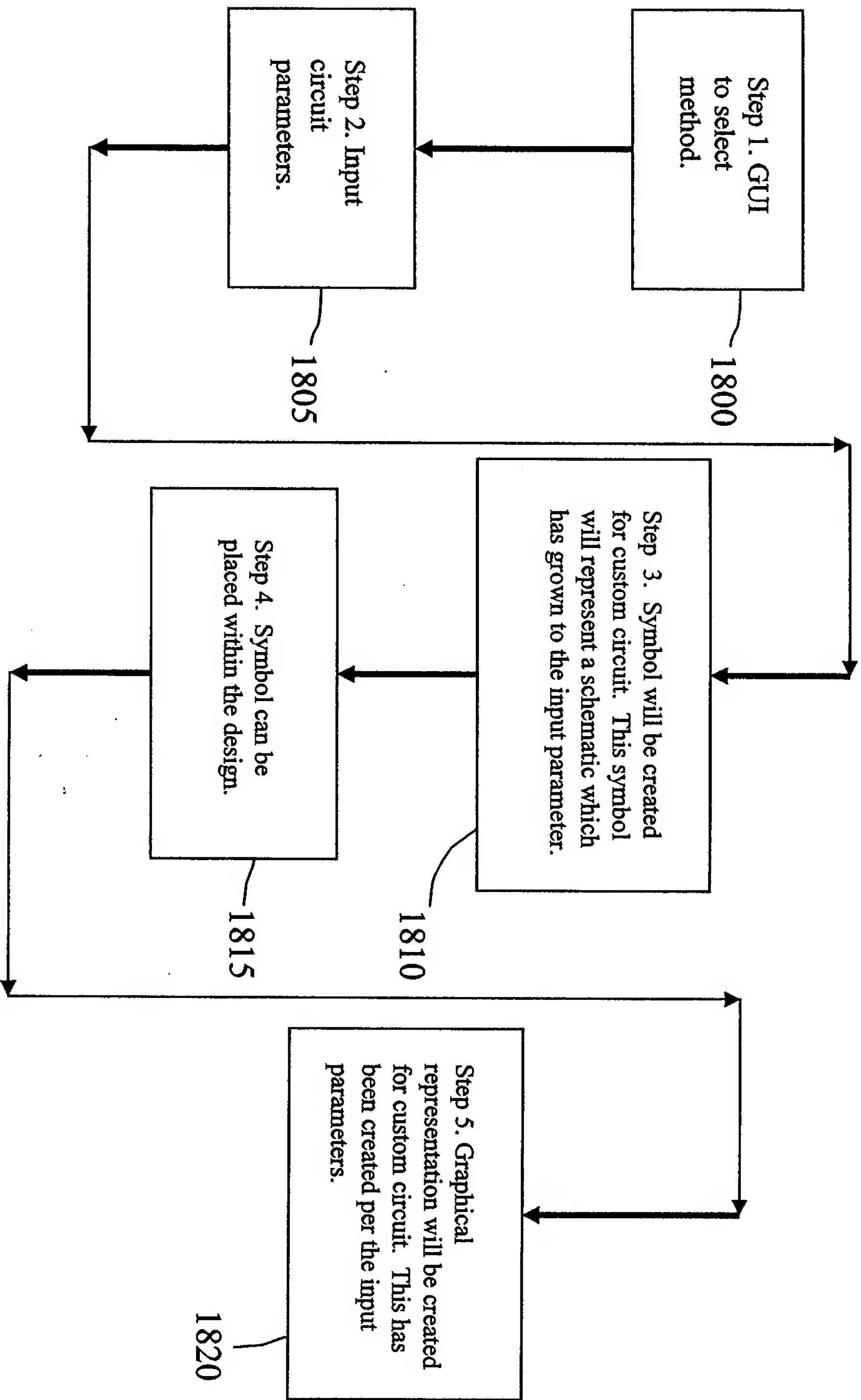


Figure 18

## Schematic Method 2

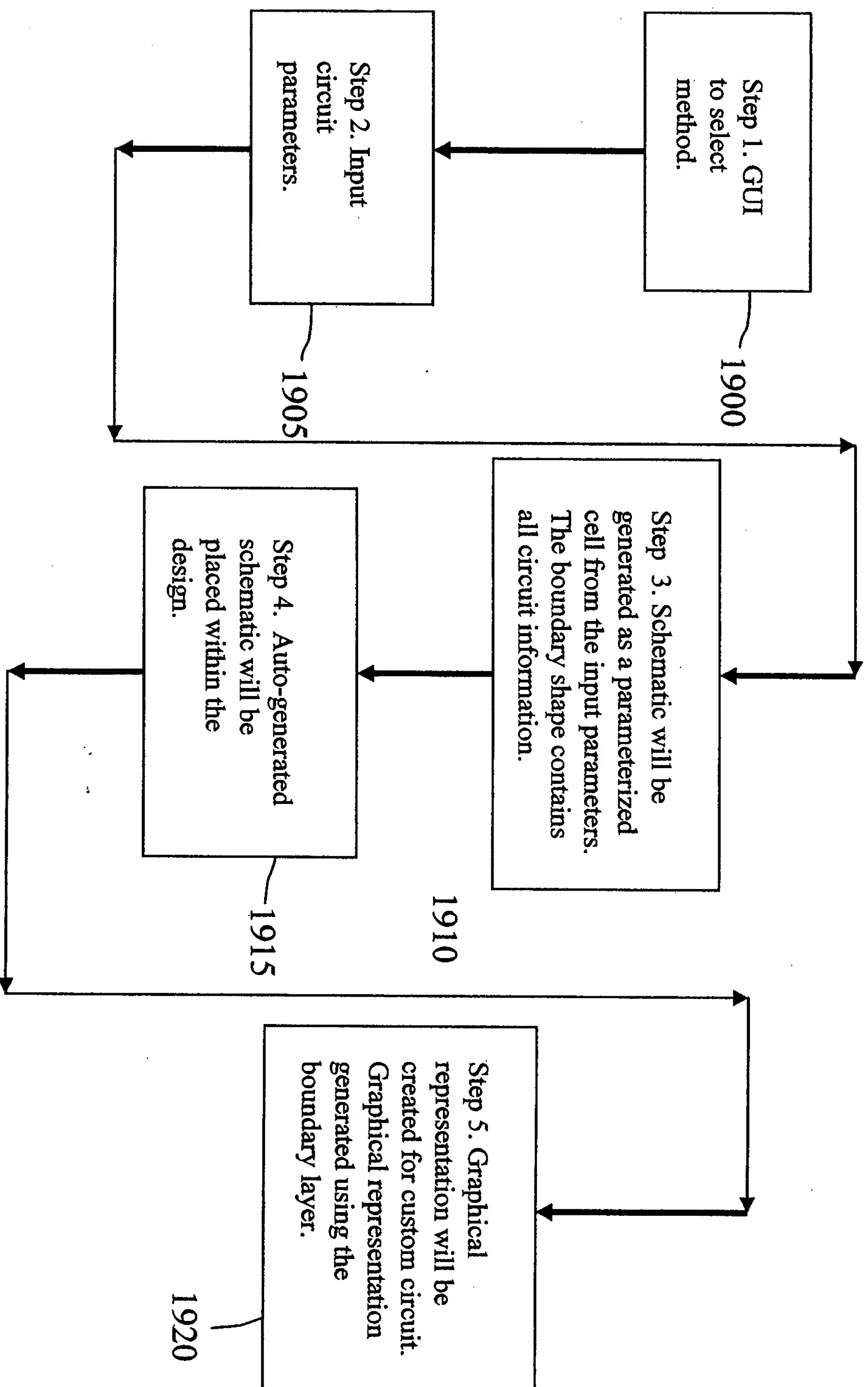


Figure 19

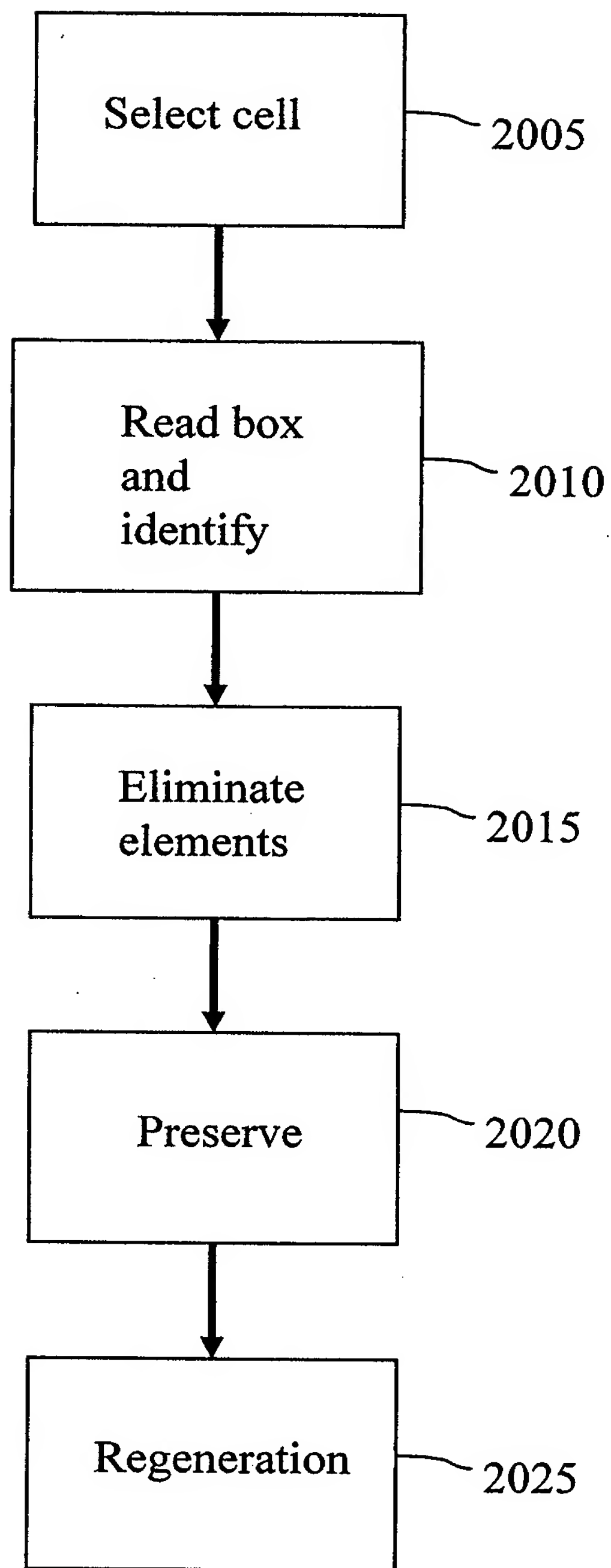


Figure 20

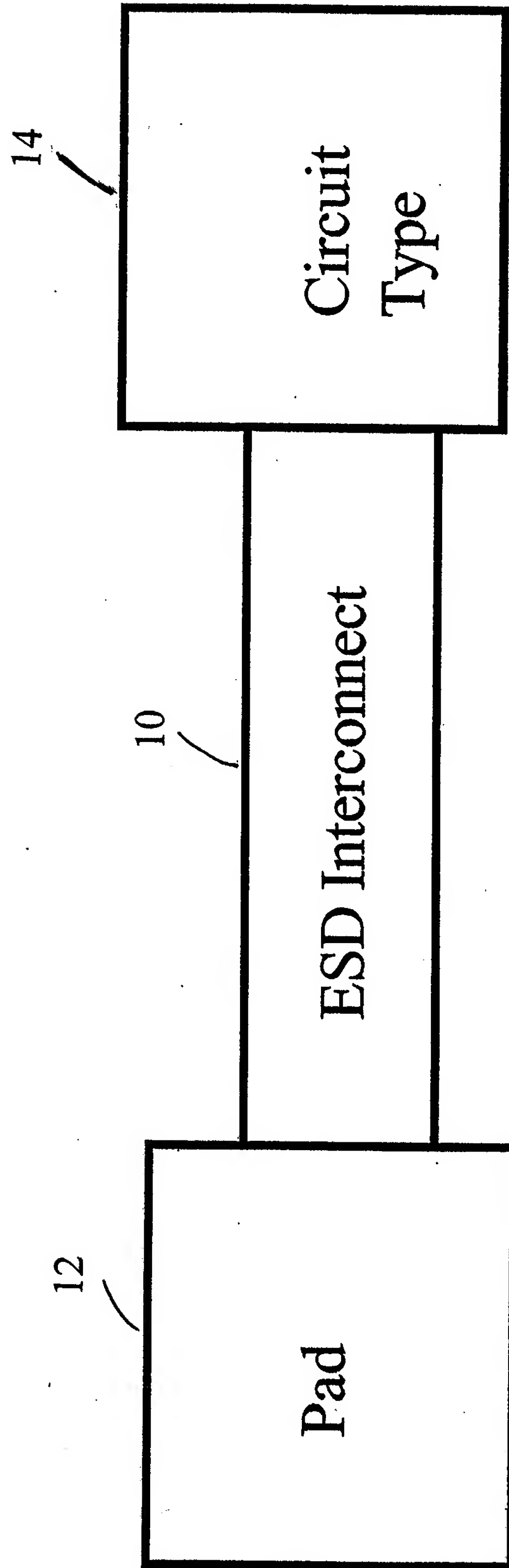


Figure 21

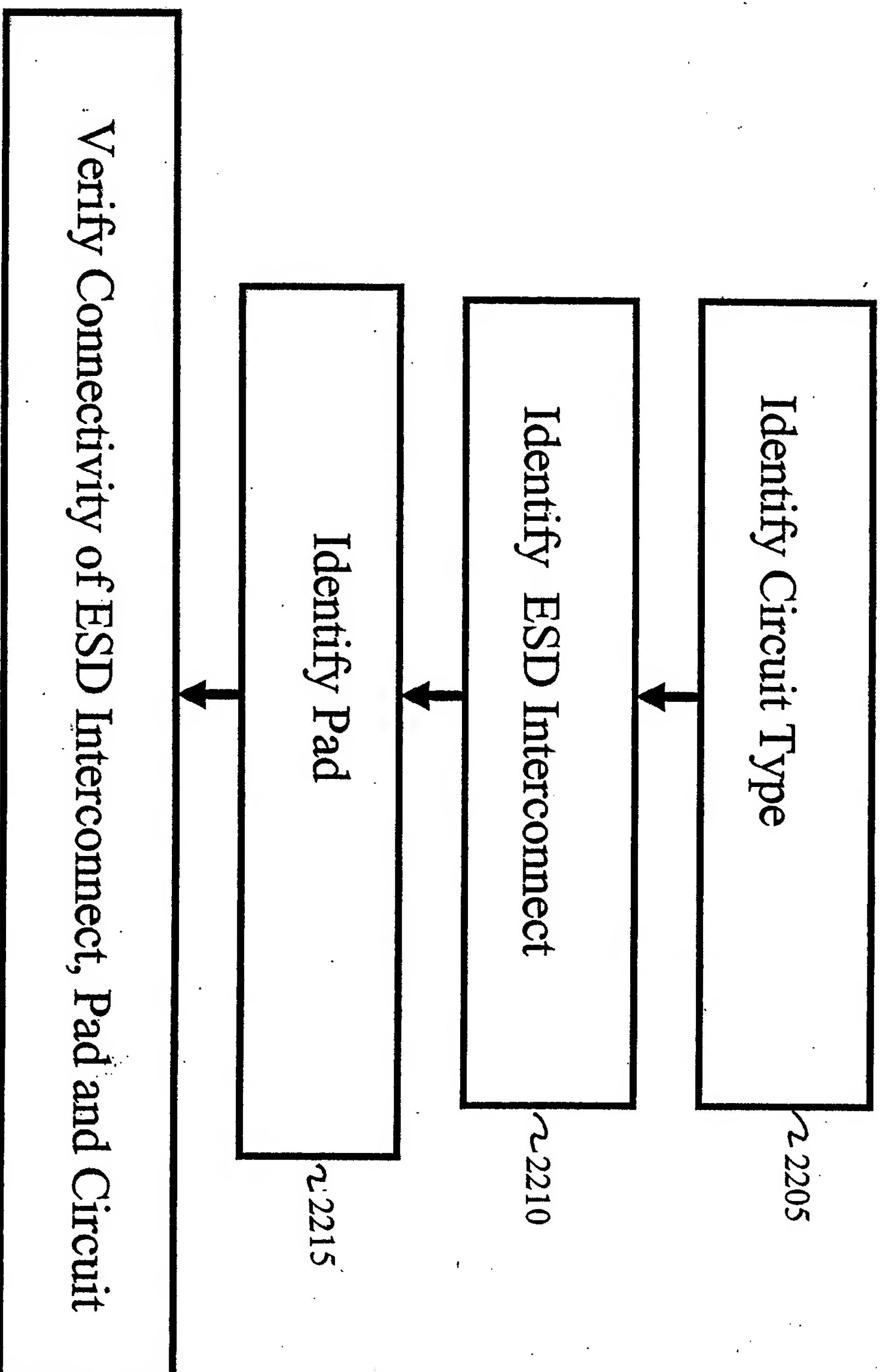


Figure 22



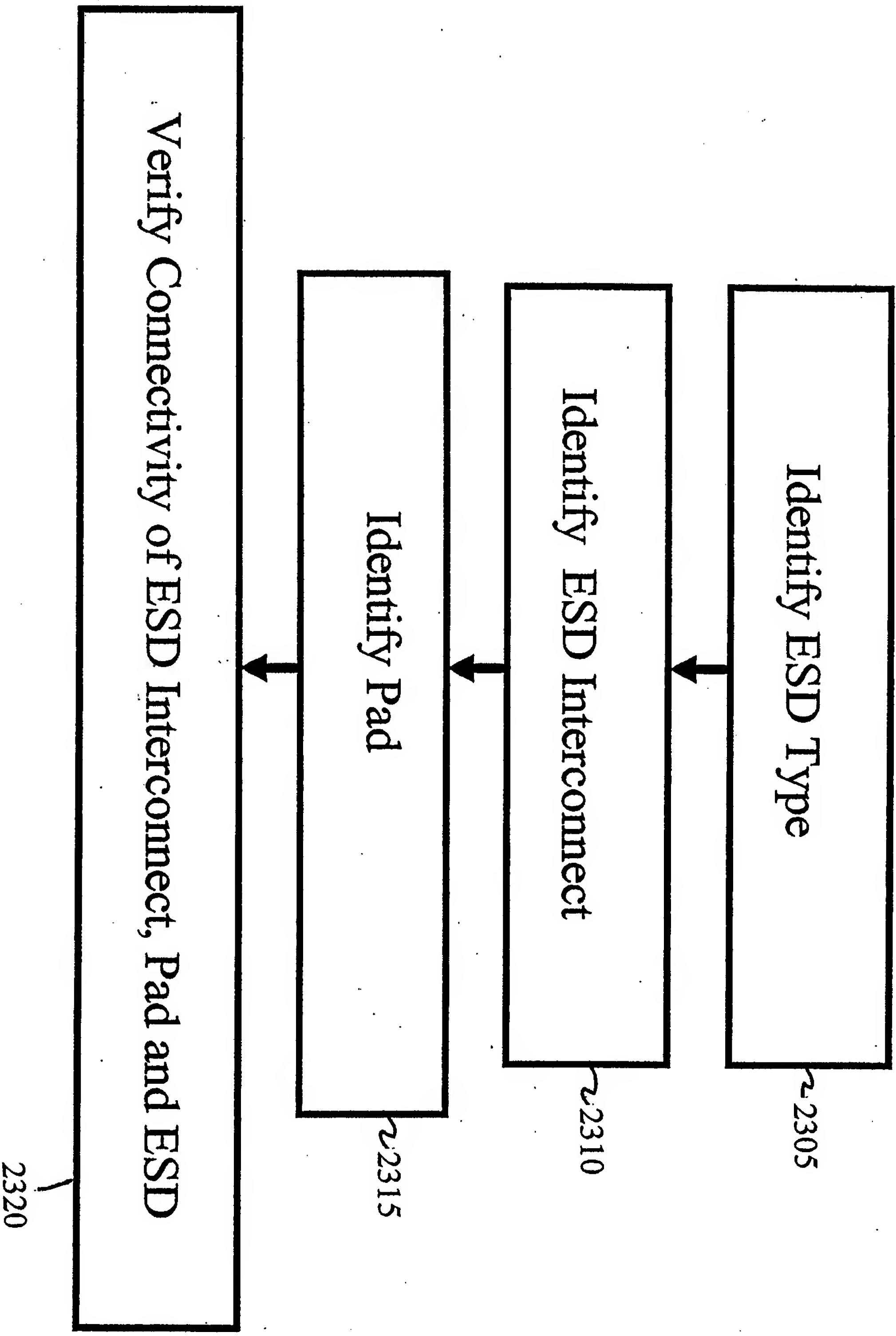


Figure 23

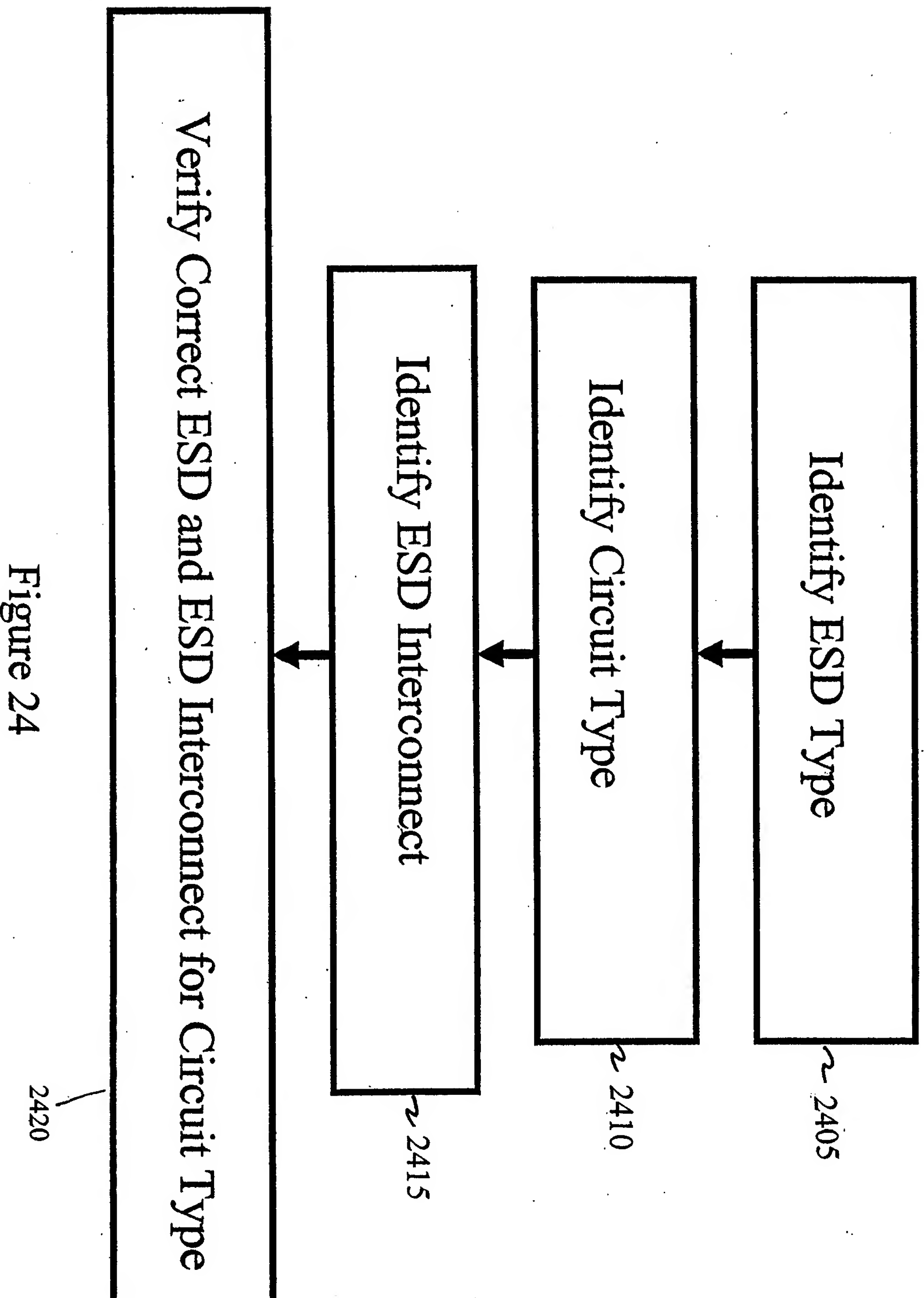


Figure 24

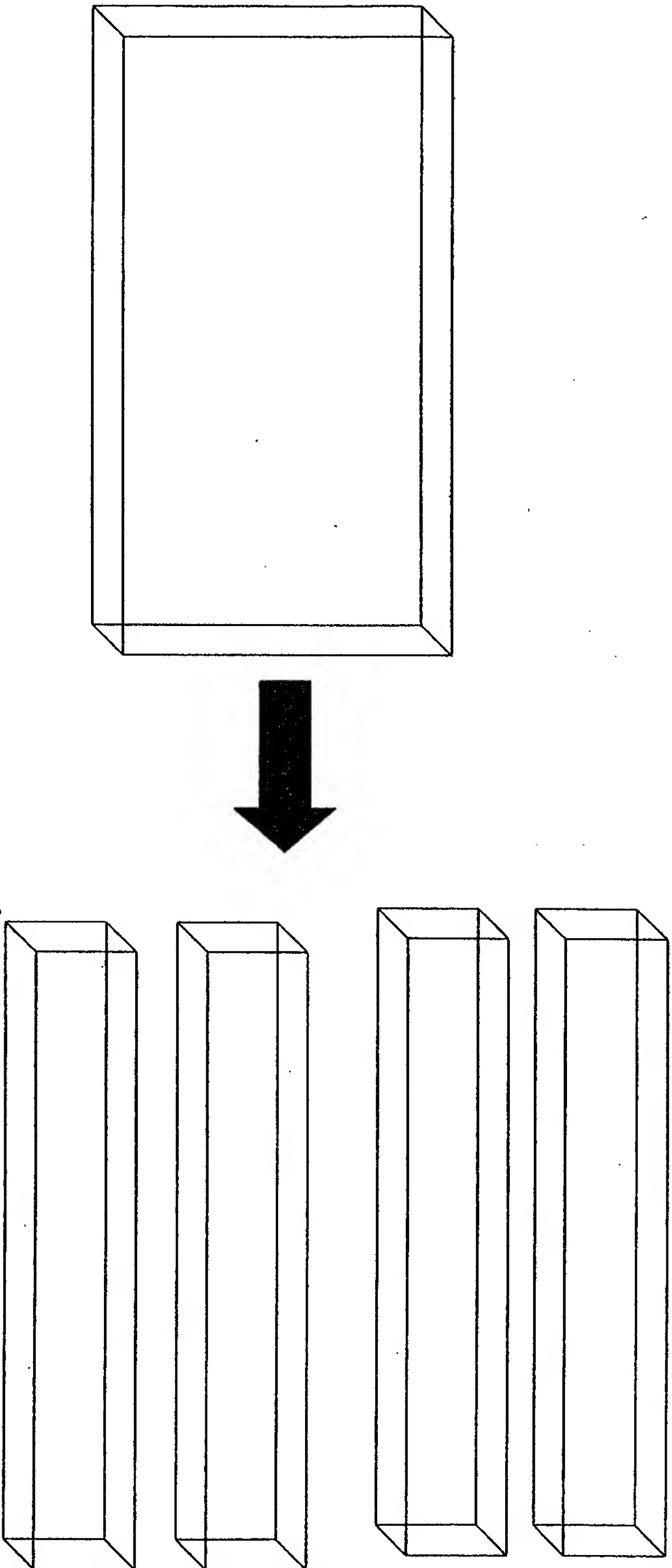
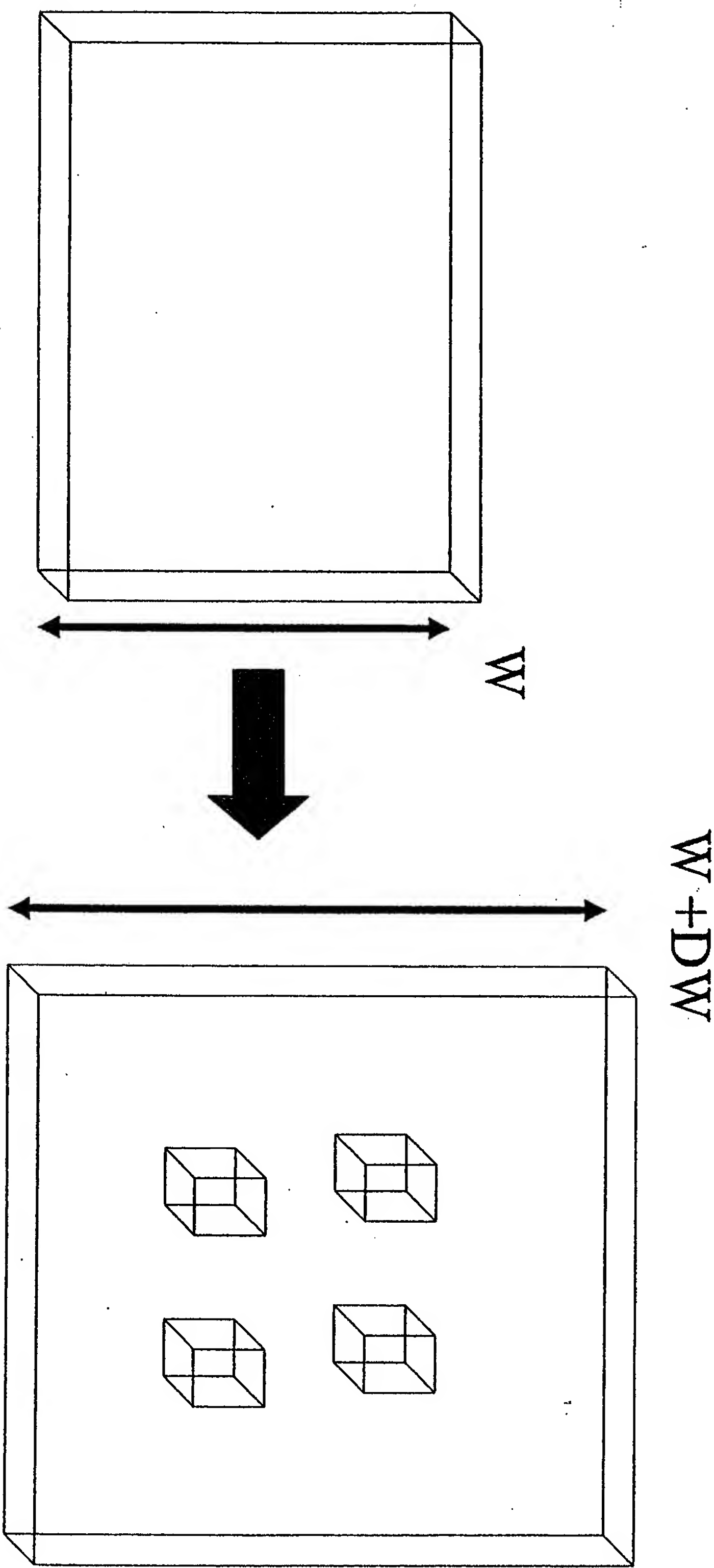


Figure 25

**ESD Interconnect P-Cell : Ballasting Feature in P-Cell  
to provide Current Uniformity**

Figure 27



ESD Interconnect P-Cell : Cheesing Feature widening of  
metal in P-Cell for ESD robustness

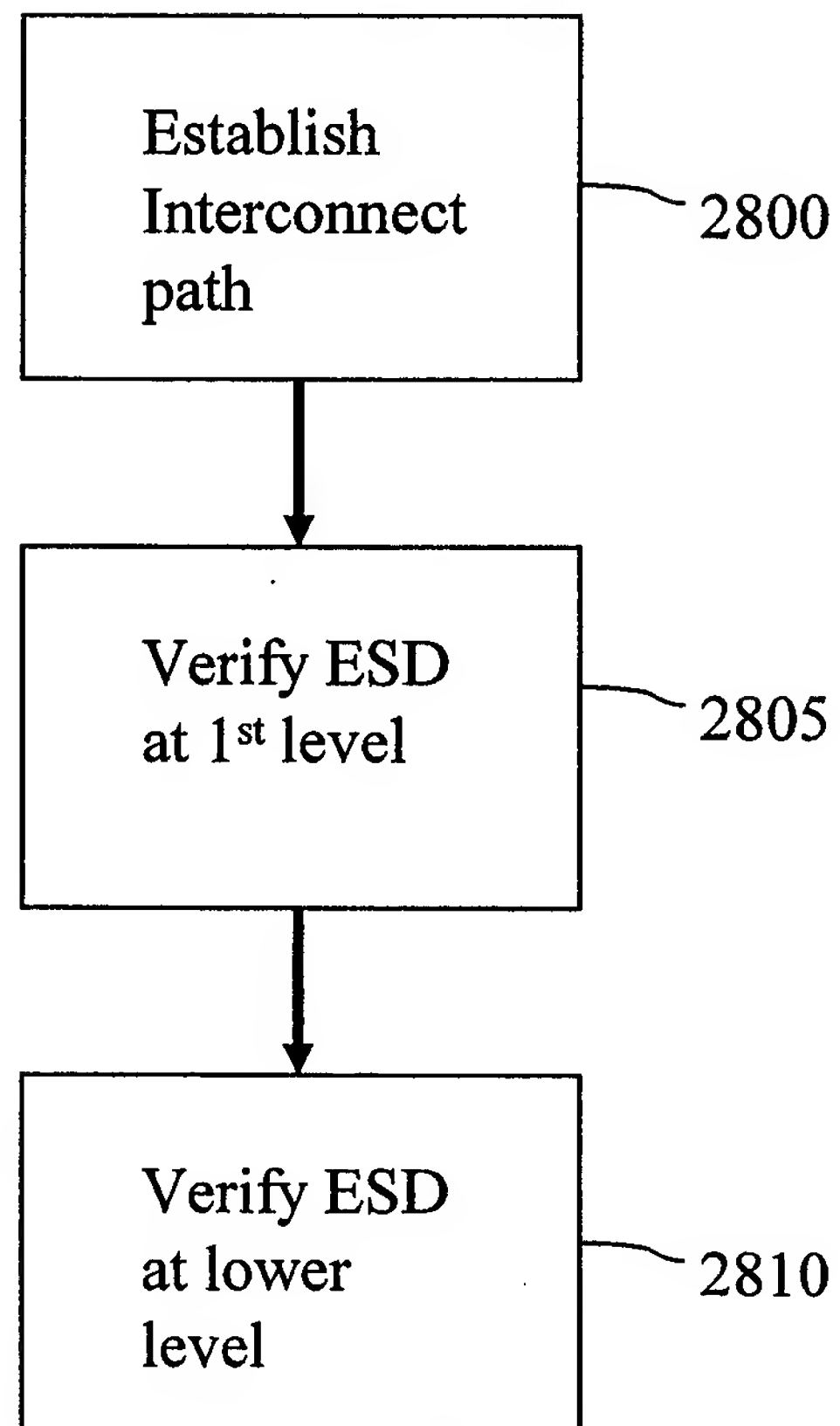


Figure 28

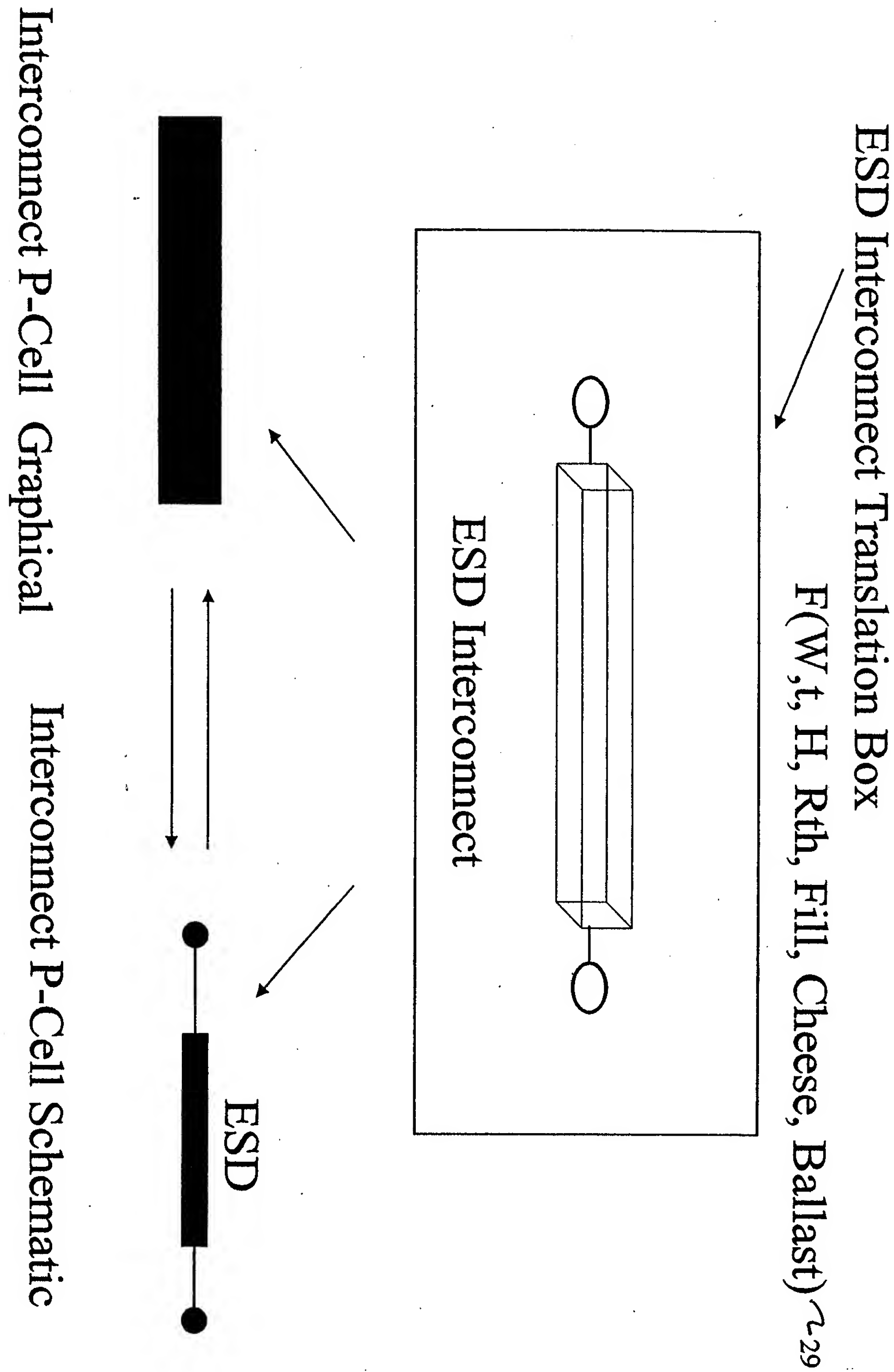


Figure 29



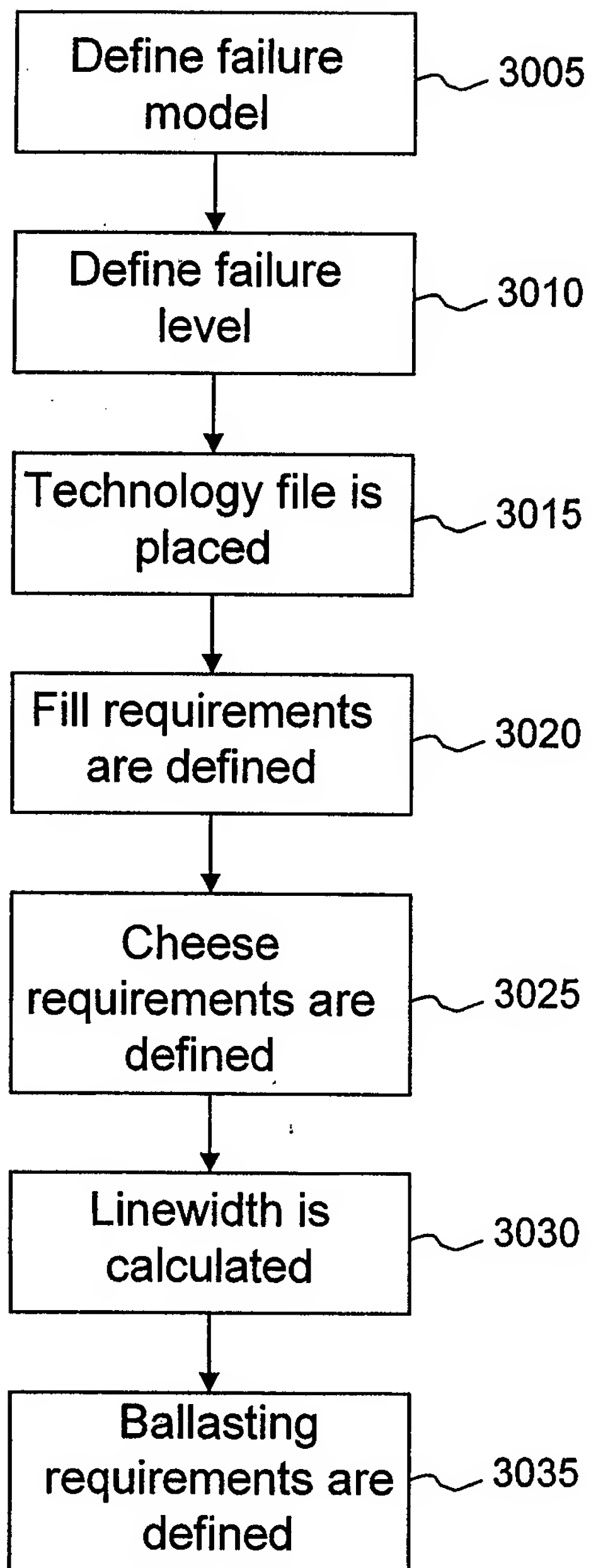


Figure 30a

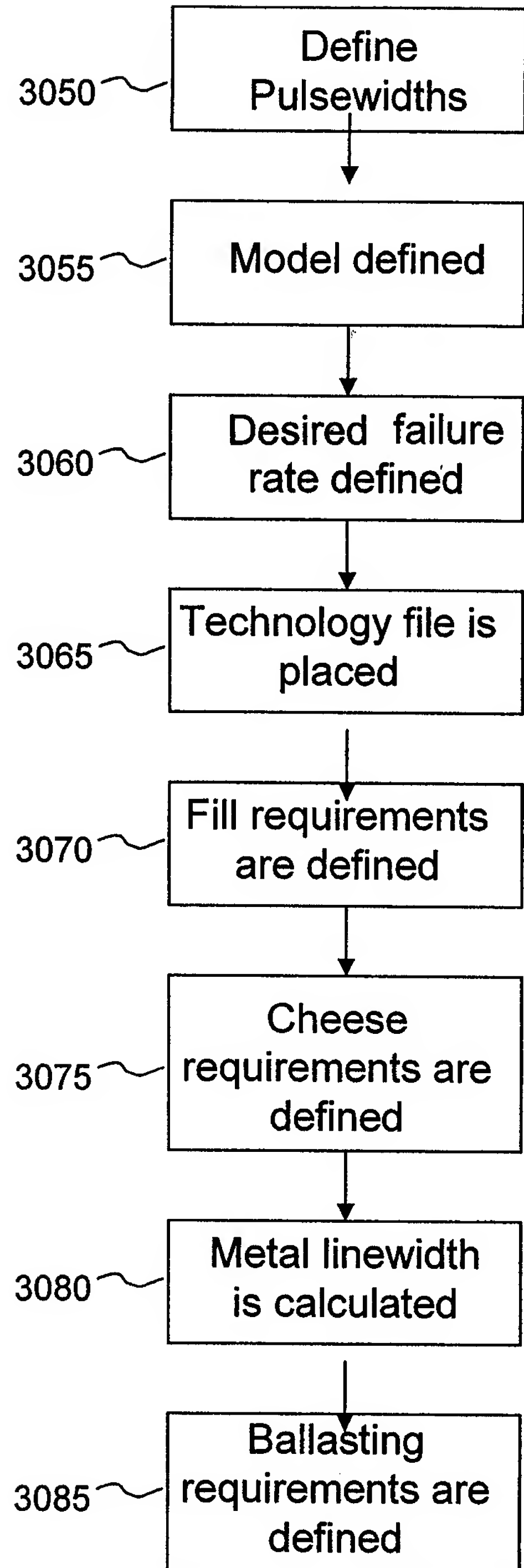


Figure 30b